

# Presettable synchronous 4-bit binary counter; asynchronous reset

## 74HC/HCT161

### FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT161 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q<sub>0</sub> to Q<sub>3</sub>) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable

input ( $\overline{PE}$ ) disables the counting action and causes the data at the data inputs (D<sub>0</sub> to D<sub>3</sub>) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for  $\overline{PE}$  are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

A LOW level at the master reset input ( $\overline{MR}$ ) sets all four outputs of the flip-flops (Q<sub>0</sub> to Q<sub>3</sub>) to LOW level regardless of the levels at CP,  $\overline{PE}$ , CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q<sub>0</sub>. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)} (CP \text{ to } TC) + t_{SU} (CEP \text{ to } CP)}$$

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> CP to TC $\overline{MR}$ to Q <sub>n</sub> $\overline{MR}$ to TC CET to TC	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	19	20	ns
			21	24	ns
			20	25	ns
			20	26	ns
			10	14	ns
f <sub>max</sub>	maximum clock frequency		44	45	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	33	35	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz  
 f<sub>o</sub> = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V
2. For HC the condition is  
 V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is  
 V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		61 22 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub>	propagation delay $\overline{\text{MR}}$ to Q <sub>n</sub>		63 23 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.9
t <sub>PHL</sub>	propagation delay $\overline{\text{MR}}$ to TC		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>w</sub>	master reset pulse width; LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9
t <sub>rem</sub>	removal time $\overline{\text{MR}}$ to CP	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.11
t <sub>su</sub>	set-up time $\overline{\text{PE}}$ to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.11

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>su</sub>	set-up time CEP, CET to CP	170 34 29	47 17 14		215 43 37		255 51 43		ns	2.0 4.5 6.0	Fig.12
t <sub>h</sub>	hold time D <sub>n</sub> , $\overline{PE}$ , CEP, CET to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	4.6 23 27	13 40 48		3.6 18 21		3.0 15 18		MHz	2.0 4.5 6.0	Fig.8